User Needs and Requirements

Sddec24-13

Project Overview

ReRam Crossbar ASIC Fabrication

- Utilize memristors to develop a crossbar matrix capable of vector matrix multiplication to perform computation

- Submit a qualifying project to Efabless using the Caravel “harness” SoC

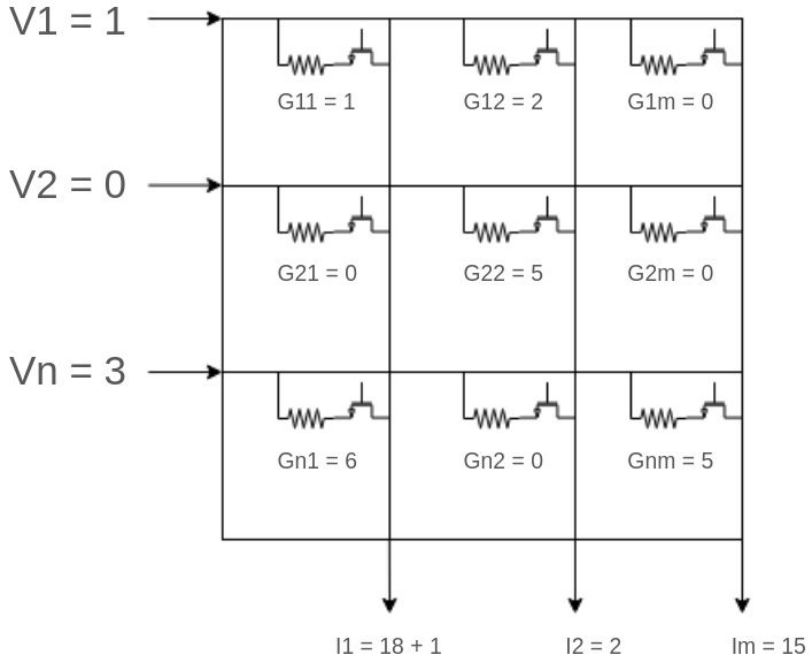
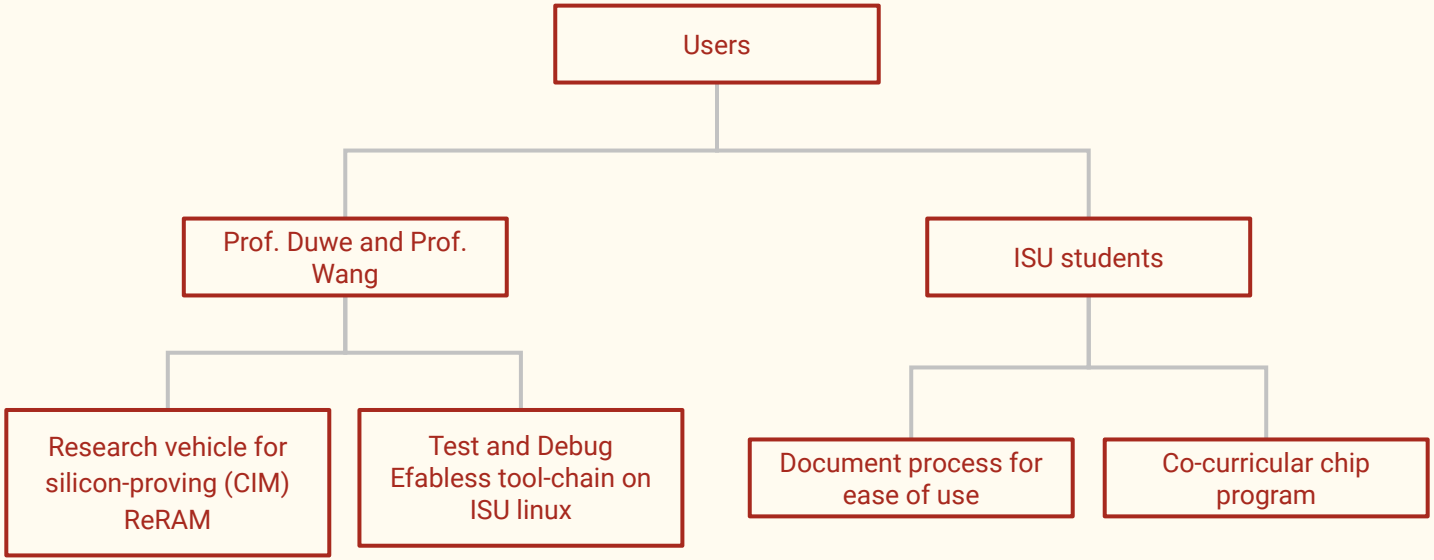


Fig 1. Example ReRam MAC

User Needs

- A research vehicle for silicon-proving computation-in-memory (CIM) ReRAM
  - Proving the ReRAM function in the analog domain
  - Designing 3 bit analog to digital converter (ADC)
  - Bit serial computation digital to analog converter (DAC)
  - Transimpedance amplifier
- Debugging of the Efabless tool-flow on ISU linux
  - Document tool-flow process for future student use(?).
- One bit shadow transistor
  - Implementation of data redundancy in case of power failure

User Needs


Users
Prof. Duwe and Prof. Wang
ISU students
Research vehicle for silicon-proving (CIM) ReRAM
Test and Debug Efabless tool-chain on ISU linux
Document process for ease of use
Co-curricular chip program

Requirements

- Validate performance of components
  a. Low overall power consumption
  b. Ensure the DAC outputs correct voltage thresholds
  c. ADC will have a higher than 1 bit resolution
  d. Low power transimpedance amplifier
- Precheck approved GS2
  a. All subcircuits need to pass Design Rule Check(DRC) and Layout Versus Schematic (LVS)
  b. Final Design must be integrated with Caravel Harness and Pass LVS
- Simulations showing correct functionality
- Bring-up plan for success/failure for chip fabrication

Engineering Standards

- IEEE 1076.4-2000 - IEEE Standard VITAL ASIC Modeling Specification
- IEEE 1481-2019 - IEEE Standard for Integrated Circuit (IC) Open Library Architecture
- IEEE 1149.4-2010 - IEEE Standard for a Mixed-Signal Test Bus
- IEEE 1364-2005 - IEEE Standard for Verilog Hardware Description Language